#3 IDS 9/19/1

SHEET 1 OF 1

Form PTO 1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY DOCKET NO. 213672US2	SERIAL NO. NEW APPLICATION
LIST OF REFERENCES CITED BY APPLICANT	APPLICANT Kenji YAMAGUCHI, et al.	
	FILING DATE HEREWITH	GROUP

09/19/01 jc978 U.S. PTO 09/955080

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	AA						
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						
	AL						
	AM						
	AN						

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	TRANSLATION YES	NO
MAF	AO	9-92700	4/4/97	Japan		X
	AP					
	AQ					
	AR					
	AS					
	AT					
	AU					
	AV					

OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, etc.)

MAF	AW	Narain D. ARORA, et al. "AN ACCURATE METHOD OF DETERMINING MOSFET GATE OVERLAP CAPACITANCE" Solid State Electronics Vol. 35, No. 12, 1992, pgs. 1817-1822
	AX	
	AY	
	AZ	

Examiner [signature]	Date Considered 6/17/2004

*Examiner: Initial if reference is considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.